RapidChip Technology Boosts IPWireless UMTS TDD Market Leadership

Time to market reduced by 60 percent, design time cut by a third, and power consumption sliced by 80 percent.

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IPW ASIC/FPGA Development Team (Dave Trewren, Steve Geers, Dave Bethune, Geert Winters, Paul Cooke, Joe Moloney)

The Opportunity

The Universal Mobile Telecommunications System Time-Division Duplexing (UMTS TDD) market is growing rapidly, and IPWireless, Inc., headquartered in San Bruno, CA, is at the pinnacle as market leader. The company's mobile broadband products provide seamless, secure mobile broadband to subscribers using the UMTS international standard. Among its offerings, IPWireless has a full portfolio of UMTS terrestrial radio access (UTRA), time-division, code division multiple access (TD CDMA, also known as TDD) Node B base stations to comply with the needs of operators with a range of business and deployment plans.

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The Node B base station is a low-cost unit designed in a small, fully environmental form-factor, suitable for use in either typical cellular sectored macrocells or indoor/outdoor microcells. Node B's can also be used in many different network architectures according to operator requirements. Coverage is dependent on network configuration and ranges about 2.5 km in a typical, suburban cellular environment to 30 km in a supercell deployment.

IPWireless is the only company with commercially deployed systems based on the UMTS TDD standard. About 15 commercial networks worldwide use these base stations with about 40 trials currently taking place around the globe.

"The technology is poised to really change the marketplace," said Madelyn Smith, Director of Communications at IPWireless. "Existing mobile cellular networks simply cannot offer the speeds and throughputs that UMTS TDD technology can. This and other major market forces are driving demand for higher bandwidth networks and that's where UMTS TDD comes in. There is a growing demand for true broadband connectivity wherever you are, not just at home, not just in the office and not just in your Starbuck's Wi-Fi hot spots. Our base stations enable that high level of connectivity."

Multi-Billion Dollar Market

According to Deutsche Bank Securities, the UMTS TDD standard represents a multi-billion dollar market opportunity. With this kind of market impetus, getting its Node B base stations out the door as fast as possible is a top priority for IPWireless design engineers.

The RapidChip *Integrator*™ Platform ASIC provided the critical boost to significantly reduce time to market and design time. Joe Moloney, technical manager for ASIC and FPGA development, said, "RapidChip technology reduced our time to market by 60 percent with design time down by a third. The next RapidChip Platform ASIC-based design we do will be faster still since we now have more experience with the RapidChip flow."

An earlier design was based on three costly and power hungry FPGAs. On top of that, the company's intellectual property (IP) was in jeopardy since SRAM-based FPGAs offer no security. "We felt vulnerable with an FPGA. There was no way to protect our IP during programming, so it can easily be ripped off. With a RapidChip platform ASIC, there's none of that," he said.

The RC11Si240 RapidChip Integrator Platform ASIC, packing 2 Mbit of RAM and 3 million gates, was used in this Node B base station design to implement transport channel processing. Here, RapidChip technology provided designers the right solution when they required high density, high performance ASICs, but still needed to achieve fast time-to- market within a design budget. RapidChip Platform ASICs fill the void between FPGAs and cell-based ASICs, but combine the best attributes of both. Those attributes include the high-density, high-performance benefits of standardcell ASICs and fast time-to-market and customization benefits of FPGAs.

The RapidChip Integrator Platform ASIC performs "a large list of tasks as part of the transport channel processing, but it basically processes data the base station is about to transmit and has received." according to Moloney. Transmit transport channel (Tx TrCH) processing includes such operations as turbo/ convolutional coding, interleaving, rate matching, scrambling, and segmentation, while receive TrCH does turbo/Viterbi decoding, de-interleaving, rate matching, de-scrambling, and desegmentation, among other operations.

Signing Up For RapidChip Platform ASIC Technology

With an FPGA-based design approach quickly becoming problematic, there may have been unspoken fleeting thoughts given to cell-based ASICs, but as Moloney put it, that route was virtually out of the question, "the timeframe didn't allow for it. We needed to get the cost down very, very quickly. LSI Logic's engineering management came in and presented this RapidChip proposal to us. We liked the sound of it; we liked the cost of it; we signed up on the spot and did the design very quickly as a result."

By taking the RapidChip technology design route, IPWireless engineers drastically cut power consumption by a third, according to John Crane, technical associate for Node B design. Those three FPGAs devoured a total of six watts, whereas the RapidChip Platform ASIC consumed only slightly more than a watt. Plus, the engineers sliced cost by about 85 percent and significantly reduced the design's bill of materials.

"From my viewpoint, the big drivers were protecting our IP and cost reduction. Those were two key reasons we went to RapidChip technology," said Adrian Stanislaus, technical manager for Node B hardware. Maintaining a small form factor and shrinking the board real estate was equally as important, he added. "We are very tight on real estate in our base stations. We would have struggled to fit the required number of FPGAs on the available area of that particular card. Replacing those big FPGAs with the one RapidChip Platform ASIC gave that area lots of breathing room."

As for the ease of design the RapidChip Platform ASIC provided, Moloney explained, "Essentially, it was a real no brainer to take our design and drop it into this LSI Logic chip. It's got a load of gates and a load of RAM and I might add, with the right amounts we needed to cover what we had in the FPGAs. It was indeed a good fit."

Lastly, the design flow proved to be highly productive and a major contributor to reducing time-to-market. Moloney said, "From my point of view, the flow was incredibly important for us. Again, part of the no brainer was the fact that we did an RTL hand-off to LSI Logic to considerably simplify our project. We're a small company with limited engineering resources, really, to do this backend stuff. If we can hand the design over at the RTL stage, we can get on and start working on our next chip."

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